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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/772,093	01/26/2001	Feng Chen	4-10	7966

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MENDELSOHN AND ASSOCIATES PC
1515 MARKET STREET
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EXAMINER	
CHANG, EDITH M	

ART UNIT	PAPER NUMBER
2637	

DATE MAILED: 01/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action	Application No.	Applicant(s)	
	09/772,093	CHEN ET AL.	
	Examiner	Art Unit	
	Edith M Chang	2637	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 22 December 2004 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE. Therefore, further action by the applicant is required to avoid abandonment of this application. A proper reply to a final rejection under 37 CFR 1.113 may only be either: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114.

PERIOD FOR REPLY [check either a) or b)]

a) ☐ The period for reply expires _____months from the mailing date of the final rejection.

b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.
ONLY CHECK THIS BOX WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

1. ☐ A Notice of Appeal was filed on _____. Appellant's Brief must be filed within the period set forth in 37 CFR 1.192(a), or any extension thereof (37 CFR 1.191(d)), to avoid dismissal of the appeal.
2. ☐ The proposed amendment(s) will not be entered because:
   (a) ☐ they raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ they raise the issue of new matter (see Note below);
   (c) ☐ they are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ they present additional claims without canceling a corresponding number of finally rejected claims.
   NOTE: _____.
3. ☐ Applicant's reply has overcome the following rejection(s): _____.
4. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
5. ☒ The a)☐ affidavit, b)☐ exhibit, or c)☒ request for reconsideration has been considered but does NOT place the application in condition for allowance because: *See Continuation Sheet*.
6. ☐ The affidavit or exhibit will NOT be considered because it is not directed SOLELY to issues which were newly raised by the Examiner in the final rejection.
7. ☒ For purposes of Appeal, the proposed amendment(s) a)☒ will not be entered or b)☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: _____.
   Claim(s) rejected: *1-20,27,31-46*.
   Claim(s) withdrawn from consideration: _____.
8. ☐ The drawing correction filed on _____ is a)☐ approved or b)☐ disapproved by the Examiner.
9. ☐ Note the attached Information Disclosure Statement(s)(PTO-1449) Paper No(s). _____.
10. ☐ Other: _____

Continuation of 5. does NOT place the application in condition for allowance because:

Regarding claims 1 and 16, applicant argues that the reference does not teach two or more sum outputs generated between consecutive shiftings of new data into the shift registers.

The reference Zhou teaches two embodiments, Fig. 3 and Fig. 23.

In Fig.3, discloses the two multiple stage shift registers, the first multiple stage shift register is R11-R1n and the second multiple stage shift register is R21-R2n. At CLK0 (i), data from the A/D (analog to digital converter) is shifted into the first multiple stage shift register R11-R1n and produce an output Aout(i) from the ADD (adder), at CLK1(i+D/2), data is shifted into the second multiple stage shift register R21-R2n and produce another output Aout(i+D/2) from the ADD, wherein the CLK 1 is shifted by half an chip time form CLK0 (column 3 lines 37-42), the D is used as to indicate one chip time for illustration/explanation purpose. At the next chip time CLK0 (2i) new data is shifted into the first multiple stage shift register R11-R1n and at CLK1 (2i+D/2) new data is shifted into the second multiple stage shift register R21-R2n, hence between consecutive shiftings (at i and 2i+D/2) of new data into the two multiple stage shift registers R11-R1n and R21-R2n, there are two sum outputs, Aout(i) and Aout(i+D/2) are generated as recited in the claims. Therefore, the reference teaches the invention recited in the claims.

In Fig.23, Zhou teaches two multiple stage shift registers SFREG1 and SFREG2 wherein the SFREG1 and SFREG2 shift the input voltages toward the last stages in response to the clock pulses CLK1 and CLK2 (column 9 lines 57-59). At CLK1(shift 1) the data from the output of the A/D is shifted into SFREG1 and produce a sum Aout(shift 1), at CLK2(shift 2) the data is shifted into SFREG2 and produce a sum Aout(shift 2) as the first embodiment (Fig.3, column 9 lines 63-67), at the next CLK1 (shift 3) new data is shifted into SFREG1 and the next CLK2 (shift 4) new data is shifted into SFREG2. Therefore, between the shift 1 and shift 4, the consecutive shiftings of new data into the SFREG1 and SFREG2, there are two sums (Aout(shift 1) & Aout(shift 1)) are generated. Hence, the reference teaches the invention as recited in the claims.
The Fig.23 was used in the previous final rejection to Claims 1 and 16.

According to the summary of the processing of Fig.3 in Zhou listed in the page 9 of the Remarks/Arguments filed on December 22, 2004, the step (1) and step (2) is the first shifting of new data into the two multiple stage registers R11-R1n and R21-R2n; and step (3) and step (4) is the second shifting of new data into two multiple stage registers R11-R1n and R21-R2n; and between these two consecutive shiftings of new data into the two multiple stage registers R11-R1n and R21-R2n (1st shifting: steps 1&2 and 2nd shifting: steps 3&4), there are two sums 1st output value (in step (1)) and 2nd output value (in step (2)) are generated. Consequently, the reference teaches the invention as recited in the claims.

Regarding claims 33 and 35, Applicants argues that in Zhou, at most a single output is generated for each loading of new data into the shift register sequences. Thus Zhou does not teach the generation of a second sum before shifting new data into first and second shift registers.
Zhou teaches that, the time duration to shifting new data into first and second shift register is the chip time (D) during which two sums are generated, one is from the first shift register and the other one is from the second shift register (refer to the response to the claims 1 and 16).

Regarding claims 38 and 46, Applicants argues that for at least some of the same reasons provided earlier, claims 38 and 46 are allowable over the cited references.
Zhou teaches all subject matter claimed in Fig.3 and Fig.23, Zhou discloses a N=2 version implementation of the invention of the current application, wherein a digital filter comprising N (N=2) multiple-stage shift register; a register adapted to store PN; multiplier; and an adder arranged as cited in the claims and each comprised element performs the function as cited in the claims.

YOUNG T. TSE
PRIMARY EXAMINER